IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Saul R. Dooley et al. Group Art Unit: 2611

Application No.: 10/564,422 Examiner: Dsouza, Joseph Francis A.

Filed: January 11, 2006 Confirmation No.: 8967

For: METHOD OF CORRELATING A SAMPLED DIRECT SEQUENCE SPREAD SPECTRUM SIGNAL WITH A LOCALLY PROVIDED REPLICA

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37(a)

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated April 28, 2009, which finally rejected claims 1-13 in the above-identified application. The Office date of receipt of Appellants' Notice of Appeal was July 23, 2009. This Appeal Brief is hereby submitted pursuant to 37 C.F.R. § 41.37(a).

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## I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the full interest in the invention, NXP B.V., of Eindhoven, Netherlands.

## II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.

## III. STATUS OF CLAIMS

No claims are canceled.

No claims are withdrawn.

No claims are objected to.

Claims 1-13 stand rejected as follows:

Claims 1, 2, 4, 6, 7, 9, and 11-13 stand rejected under 35 U.S.C. 102(b) as being anticipated by Medlock (U.S. Pub. Pat. No. 2001/0048713, hereinafter Medlock).

Claims 3 and 8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Medlock in view of Laudel et al. (U.S. Pat. No. 6,657,986, hereinafter Laudel).

Claims 5 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Medlock in view of Harrison et al. (U.S. Pat. No. 5,982,811, hereinafter Harrison).

Claims 1-13 are the subject of this appeal. A copy of claims 1-13 is set forth in the Claims Appendix.

## IV. STATUS OF AMENDMENTS

There were no proposed amendments to the claims submitted subsequent to the Final Office Action mailed April 28, 2009.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

This section of this Appeal Brief is set forth to comply with the requirements of 37 C.F.R. § 41.37(c)(1)(v) and is not intended to limit the scope of the claims in any way. Examples of implementations of the limitations of independent claims 1 and 6 are described below.

The language of claim 1 relates to a method of correlating a sampled direct sequence spread spectrum signal with a locally provided replica signal containing a spreading code. Specification, page 2, lines 10-14. The method includes combining the bit or bits of at least two signal samples of the received signal to form a first word. Specification, page 4, lines 14-18. The method also includes providing a second word containing bits corresponding to the replica signal. Id. The method also includes executing one or more software based instructions to carry out word-based, hard-wired operations to process the first and second words in order to obtain a correlation value. Specification, page 4, lines 18-23.

The language of claim 6 relates to a signal processor configured for correlating a sampled direct sequence spread spectrum signal with a locally provided replica signal containing a spreading code. Specification, page 2, lines 10-14. The signal processor functions to combine the bit or bits of at least two signal samples of the received signal to form a first word. Specification, page 4, lines 14-18. The signal processor also functions to provide a second word containing bits corresponding to the replica signal. Id. The signal processor also functions to execute one or more software based instructions to carry out word-based, hard-wired operations to process the first and second words in order to obtain a correlation value. Specification, page 4, lines 18-23.

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1, 2, 4, 6, 7, 9, and 11-13 are patentable over Medlock under 35 U.S.C. 102(b).

B. Whether claims 3 and 8 are patentable over the combination of Medlock and Laudel under 35 U.S.C. 103(a).

C. Whether claims 5 and 10 are patentable over the combination of Medlock and Harrison under 35 U.S.C. 103(a).

## VII. ARGUMENT

For the purposes of this appeal, claims 1, 2, 4, 6, 7, 9, and 11-13 are argued together as a group for purposes of the question of patentability over Medlock under 35 U.S.C. 102(b). Claims 3 and 8 are argued together as a separate group for purposes of the question of patentability over the combination of Medlock and Laudel under 35 U.S.C. 103(a). Claims 5 and 10 are argued together as a separate group for purposes of the question of patentability over the combination of Medlock and Harrison 35 U.S.C. 103(a).

A. Claims 1, 2, 4, 6, 7, 9, and 11-13 are patentable over Medlock because Medlock does not disclose all of the limitations of the claims.

Appellants respectfully assert that claim 1 is patentable over Medlock because Medlock does not disclose all of the limitations of the claim. Claim 1 recites:

> A method of correlating a sampled direct sequence spread spectrum signal with a locally provided replica signal containing a spreading code, the method comprising:
>
> combining the bit or bits of at least two signal samples of the received signal to form a first word;
>
> providing a second word containing bits corresponding to the replica signal; and
>
> executing one or more software based instructions to carry out word-based, hard-wired operations to process the first and second words in order to obtain a correlation value.
>
> (Emphasis added.)

In contrast to the language of the claim, Medlock does not disclose all of the limitations of the claim because Medlock does not disclose carrying out word-based, hard-wired operations to process first and second words in order to obtain a correlation value.

For reference, it may be useful to clarify the general argument presented in Appellants' previous responses. In the Advisory Action mailed July 1, 2009, the Examiner characterizes Appellants' arguments as including two separate arguments: 1) Medlock does not disclose word-based processing, and 2) Medlock does not disclose that the multiplication process is performed in parallel. However, Appellants have not argued the second point raised by the Examiner. Rather, Appellants' previous arguments and the arguments presented herein specifically relate to the failure of Medlock to disclose word-based processing. To the extent that the multiplication of Medlock might be discussed herein, such discussion is merely presented in support of the argument that Medlock does not disclose word-based processing, because the description in Medlock of implementing chip- or bit-based multiplication operations in parallel nevertheless fails to disclose word-based processing, as explained below.

Although Medlock describes a process of performing parallel searches for a phase offset between first and second signals (Medlock, paragraph 27, lines 4-6), Medlock expressly states that the sub-steps used in the correlation process are implemented one chip at a time (Medlock, paragraph 50, lines 8-10). In direct-sequence spread spectrum (DSSS) coding such as code division multiple access (CDMA) techniques described in Medlock, a chip is essentially analogous to a bit. Thus, the description in Medlock of processing one chip at a time is at best analogous to processing one bit at a time.

The description in Medlock of processing one chip or bit at a time is insufficient to disclose word-based processing because processing one chip or bit at a time does not describe or enable processing multiple bits at the same time. Since processing one chip or bit at a time is not the same word-based processing, Medlock does not disclose all of the limitations of the claim.

Furthermore, the assertion in the Office Action mailed April 28, 2009, regarding the description of processing bits in parallel also fails to address word-based processing, as recited in the claim. The Office Action states:

> Medlock clearly states in [0043] (lines 7-9) that the bits can be processed (i.e. multiplied) in parallel.
>
> Office Action, 4/28/09, page 2 (emphasis added).

For reference, the cited portion of Medlock states:

> If multiply circuit performs its multiply operations for each of the chips in the first signal and the second signal in parallel, then integrate circuit 306 utilizes an address tree in memory to sum the results.
>
> Medlock, paragraph 43, lines 7-9 (emphasis added).

This reference to the multiply circuit refers to the multiply circuit 304 shown in Fig. 3 of Medlock. In regard to the multiply circuit 304, Medlock merely describes multiplying chips or bits of a first sequence with chips or bits of a second sequence. Medlock, paragraph 42, lines 8-12. More specifically, Medlock describes a multiply-logic device for parallel operations on a chip-by-chip basis. Medlock, paragraph 42, lines 12-14. Thus, all of the operations performed are chip- or bit-based operations. Additionally, Medlock describes multiple multiply-logic devices for multiplying both an in-phase (I) and quadrature-phase (Q) chip of a first code sequence with an appropriate I phase portion and a Q phase chip of a second code sequence. Medlock, paragraph 42, lines 17-22.

Even though Medlock describes the possibility of processing certain bits in parallel, the description in Medlock of processing bits in parallel nevertheless fails to disclose the actual limitations of the claim because Medlock does not disclose word-based processing. At best, Medlock merely describes bit-based processing for a first signal and separate bit-based processing for a second signal. In other words, two signals are processed in parallel on a chip-by-chip or bit-by-bit basis.

However, processing two separate signals (or replicas of a signal) in parallel on a bit-by-bit basis is not the same as word-based processing because the separate chips or bits from separate signals do not constitute a word, even if they are processed in parallel. Rather, the separate processing of separate signals on a bit-by-bit basis nevertheless remains bit-by-bit processing, even though separate signals are processed in parallel. Therefore, the description in Medlock of bit-by-bit processing of separate signals in

parallel is insufficient to disclose word-based processing and, more specifically, carrying out word-based, hard-wired operations to process first and second words in order to obtain a correlation value.

Additionally, the assertion in the Advisory Action regarding parallel chips interpreted as one bit value combined to form a word also fails to address word-based processing, as recited in the claim. The Advisory Action states:

> The chips are [sic] parallel are interpreted as one bit values [sic] combined to form a word.
> Office Action, 4/28/09, page 2 (emphasis added).

It appears that the Examiner's position is that combining chips together can be characterized as a word and, hence, processing chips is purportedly the same as processing words. However, this assertion overlooks the specific teachings of Medlock which describe processing on a chip-by-chip or bit-by-bit basis. Even though Medlock describes bit slices of an input signal (Medlock, paragraph 29; Fig. 2A, slices 203a-d) and corresponding computation circuits (Medlock, Fig. 2A, circuits 204-1 through 204-N), Medlock nevertheless specifically describes performing chip-by-chip or bit-by-bit processing within the computation circuits. Medlock, paragraph 42. The possibility that different computation circuits may perform separate bit-by-bit processing on disparate replicas of the input data 208 does not change the fact that each of the computation circuits merely performs chip-by-chip or bit-by-bit multiplication operations. Therefore, the description in Medlock of bit-by-bit processing of separate signals in parallel using different computation circuits is insufficient to disclose word-based processing and, more specifically, carrying out word-based, hard-wired operations to process first and second words in order to obtain a correlation value.

For the reasons presented above, Medlock does not disclose all of the limitations of the claim because Medlock does not disclose carrying out word-based, hard-wired operations to process first and second words in order to obtain a correlation value, as recited in the claim. Accordingly, Appellants respectfully assert claim 1 is patentable over Medlock because Medlock does not disclose all of the limitations of the claim.

Appellants respectfully assert independent claim 6 is patentable over Medlock at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Claim 6 recites similar subject matter as claim 1. Although the language of claim 6 differs from the language of claim 1, and the scope of claim 6 should be interpreted independently of claim 1, Appellants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 6.

Given that claims 2-5 and 7-13 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 6, which are patentable over the cited reference, Appellants respectfully submit that dependent claims 2-5 and 7-13 are also patentable over the cited reference based on allowable base claims. Additionally, each of claims 2-5 and 7-13 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 1, 2, 4, 6, 7, 9, and 11-13 under 35 U.S.C. 102(b) be withdrawn.

B. Claims 3 and 8 are patentable over Medlock and Laudel because the combination of cited references does not teach all of the limitations of the claims.

Given that claims 3 and 8 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 6, which are patentable over Medlock, Appellants respectfully submit that dependent claims 3 and 8 are also patentable over the combination of cited references based on allowable base claims. Additionally, each of claims 3 and 8 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 3 and 8 under 35 U.S.C. 103(a) be withdrawn.

C. Claims 5 and 10 are patentable over Medlock and Harrison because the combination of cited references does not teach all of the limitations of the claims.

Given that claims 5 and 10 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 6, which are patentable over Medlock, Appellants respectfully submit that dependent claims 5 and 10 are also patentable over the combination of cited references based on allowable base claims. Additionally, each of claims 5 and 10 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 5 and 10 under 35 U.S.C. 103(a) be withdrawn.

## VIII. CONCLUSION

For the reasons stated above, claims 1-13 are patentable over the cited references. Thus, the rejections of claims 1-13 should be withdrawn. Appellants respectfully request that the Board reverse the rejections of claims 1-13 under 35 U.S.C. 102(b) and 103(a) and, since there are no remaining grounds of rejection to be overcome, direct the Examiner to enter a Notice of Allowance for claims 1-13.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/mark a. wilson/

Date: September 23, 2009

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## IX. CLAIMS APPENDIX

1. A method of correlating a sampled direct sequence spread spectrum signal with a locally provided replica signal containing a spreading code, the method comprising:

combining the bit or bits of at least two signal samples of the received signal to form a first word;

providing a second word containing bits corresponding to the replica signal; and

executing one or more software based instructions to carry out word-based, hard-wired operations to process the first and second words in order to obtain a correlation value.

2. A method according to claim 1 wherein the processing of the first and second words is done using hardwired circuitry.

3. A method according to claim 1 wherein the processing of the first and second words includes a word based XOR operation or its inverse and a summation of the results of that operation.

4. A method according to claim 1 wherein a software based instruction is executed to form the first word.

5. A method according to claim 1 wherein each sample of the spread spectrum signal contains at least one magnitude bit and a sign bit; wherein the first word is formed by combining the magnitude bit or bits of at least two signal samples; wherein a third word is formed by combining the sign bit of at least two signal samples; and wherein one or more software based instructions are executed to process the first, second and third words in order to obtain a correlation value.

6. A signal processor configured for correlating a sampled direct sequence spread spectrum signal with a locally provided replica signal containing a spreading code by combining the bit or bits of at least two signal samples of the received signal to form a

first word, providing a second word containing bits corresponding to the replica signal, and executing one or more software based instructions to carry out word-based, hard-wired operations to process the first and second words in order to obtain a correlation value.

7. A signal processor according to claim 6 wherein the processing of the first and second words is done using hardwired circuitry.

8. A signal processor according to claim 6 wherein the processing of the first and second words includes a word based XOR operation or its inverse and a summation of the results of that operation.

9. A signal processor according to claim 6 wherein a software based instruction is executed to form the first word.

10. A signal processor according to claim 6 wherein each sample of the spread spectrum signal contains at least one magnitude bit and a sign bit; wherein the first word is formed by combining the magnitude bit or bits of at least two signal samples; wherein a third word is formed by combining the sign bit of at least two signal samples; and wherein one or more software based instructions are executed to process the first, second and third words in order to obtain a correlation value.

11. A direct sequence spread spectrum signal receiver comprising an antenna and an RF front-end including an analogue to digital converter for receiving spread spectrum signals and outputting corresponding signal samples; and a signal processor according to claim 6.

12. A computer-readable storage medium having recorded thereon data containing instructions for performing a method according to claim 1.

13. A computer program comprising instructions stored on a memory device which, when executed by a processor, perform the method according to claim 1.

## X. EVIDENCE APPENDIX

There is no evidence submitted with this Appeal Brief.

## XI. RELATED PROCEEDINGS APPENDIX

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.